REMARKS

The Examiner's Office Action of August 12, 2004 has been received and its contents reviewed. Applicant would like to thank the Examiner for the consideration given to the above-identified application, and for indicating the allowance of claims 17-20.

Claims 1-25 are pending for consideration, of which claims 1, 5, 9, 13, 17 and 21 are independent. In view of the following remarks, reconsideration of this application is now requested.

Referring now to the detailed Office Action, claims 1, 2 and 4 stand rejected under 35 U.S.C. §102(e) as anticipated by Borel et al. (U.S. Patent No. 6,297,093 hereafter Borel). Further, claims 3, 5-8 and 11 stand rejected under 35 U.S.C. §103(a) as unpatentable over Borel in view of Murai (U.S. Patent No. 5,473,184 – hereafter Murai. Still further, claims 9-10 and 12 stand rejected under 35 U.S.C. §103(a) as unpatentable over Borel in view of Papadas et al. (U.S. Patent No. 5,687,113 – hereafter Papadas). Still further, claims 13-16 stand rejected under 35 U.S.C. §103(a) as unpatentable over Borel in view of Murai and Papadas. Finally, claims 21-23 and 25 stand rejected under 35 U.S.C. §103(a) as unpatentable over Liang (U.S. Patent No. 6,180,502 – hereafter Liang) in view of Papadas. Claim 24 is objected to as dependent upon a rejected base claim. Applicant respectfully traverses the rejections and objection at least for the reasons provided below.

With respect to the §102(b) rejection, Applicant respectfully asserts that Borel does not show the steps of "forming a semiconductor film over a substrate" and " adding a second impurity to the semiconductor film while using the gate electrode and the sidewall as masks" as alleged by the Examiner. The Examiner alleges that Fig. 2C discloses a step of adding a second impurity 29. However, element 29 is a drain region as disclosed in col. 2, line 60 of Borel. Moreover, Fig. 2C of Borel is described in col. 2, lines 47-63 as follows:

> *At a subsequent step shown in FIG. 2C, thin layer 21 of conductive material is removed wherever it is not covered with spacers 23 and 24 to only leave in place L-shaped regions 25 and 26. This removal may be performed by prolonging the etching performed to form spacers 23 and 24. Preferably, the step of FIG. 2C is followed by an oxidation step to oxide the apparent surfaces of L-shaped regions 25 and 26 forming a floating gate and make them insulating. This is possible if the conductive material forming layer 21 is an oxidizable material such as polysilicon or a properly chosen metal, for example,*

> *aluminum. This insulation by oxidation avoids any short-circuiting with subsequently formed metallizations. The formation of drain and source regions 28 and 29 has also been shown in FIG. 2C. Drain, source, and control gate contacts will then be conventionally made.*

Clearly, there is no disclosure in Borel of any steps related to adding a second impurity whatsoever. Consequently, since each and every feature of the present claims is not taught (and is not inherent) in the teachings of Borel, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1, 2 and 4, under 35 U.S.C. §102(b), as anticipated by Borel, is improper.

With respect to the §103(a) rejection of claims 3 and 5-16 in which Borel is applied as the primary reference, the arguments set forth above in relation to the §102(b) rejection are also applicable. For example, with respect to claim 3, since Borel does not teach, disclose or suggest adding a second impurity, the combination of Borel with Murai still does not teach, disclose or suggest all of Applicant's claimed steps. Hence, a *prima facie* case of obviousness has not been established in the rejection of claim 3.

With respect to the rejection of claims 21-23 and 25 and the objection to claim 24, the Examiner alleges that Liang discloses "forming a sidewall 4400 to a side surface of the gate electrode in a condition of the gate insulating film 407 being covered by the conductive film (underneath the gate electrode 4200)". However, Applicant respectfully asserts that there is no such teaching, disclosure, or suggestion in Liang.

Further, as the Examiner has acknowledged, Liang lacks the step of removing the sidewall. To cure this deficiency, the Examiner cited Papadas as teaching a step of removing the side wall. However, it is well settled that when combining the references in order to support a *prima facie* case of obviousness, the references must be considered in their entirety. It is further settled that the mere fact that the prior art may be modified to reflect features of the claimed invention does not make the modification, and hence the claimed invention obvious, unless the desirability of such modification is suggested by the prior art itself (MPEP §2141). The Examiner has failed to show why the sidewall of Liang would or should be removed. The fact that Papadas merely teaches removing a sidewall does not in any way automatically mean that Liang's sidewall should also be removed. The Examiner also fails to take into consideration that, if the sidewall of Liang were removed, the intended structure,

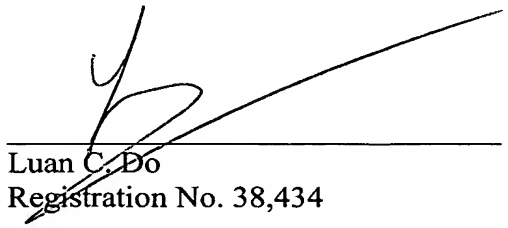
process and function of the FET of Liang would be altered. Therefore, without proper suggestion or motivation to combine the teaching of Liang with that of Papadas, the combination of their respective teachings would not make Applicant's claimed invention. Further, the combination of these references in the rejection of claims 21-23 and 25 and the objection to claim 24 are improper.

As disclosed on page 5, lines 4-18, of the present specification, for example, Applicant's claimed invention is advantageous in that a semiconductor device can form an LDD region in a self-aligning manner and minimize damage by plasma and doping process and that damage caused by charge particles during a process of adding a high concentration of impurity for a source and a drain regions formation is prevented. Applicant respectfully submits that the cited prior art references do not recognize these advantages of Applicant's claimed invention and hence do not teach, disclose, or suggest Applicant's claimed features.

In view of the amendments and arguments set forth above, Applicant respectfully requests reconsideration and withdrawal of all the pending rejections.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicant's representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby by expedited.

Respectfully submitted,



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